CLAIMS

We Claim:

1. A pre-metal dielectric structure for a silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor comprising:

a first pre-metal dielectric layer located over the SONOS memory transistor;

a light-absorbing structure located over the first-pre-metal dielectric layer;

a second pre-metal dielectric layer located over the light-absorbing structure; and

a first metal layer located over the second pre-metal dielectric layer.

2. The pre-metal dielectric structure of Claim 1, further comprising a barrier film located between the SONOS memory transistor and the first pre-metal dielectric layer.

3. The pre-metal dielectric structure of Claim 2, wherein the barrier film comprises silicon nitride.

4. The pre-metal dielectric structure of Claim 1, wherein the light-absorbing structure comprises a continuous layer of polycrystalline silicon .

5. The pre-metal dielectric structure of Claim 1, wherein the light-absorbing structure comprises a first patterned layer of polycrystalline silicon.

6. The pre-metal dielectric structure of Claim 1, wherein the light-absorbing structure comprises a first patterned layer of polycrystalline silicon.

7. The pre-metal dielectric structure of Claim 6, wherein the light-absorbing structure further comprises:

a second patterned layer of polycrystalline silicon; and

an intermediate pre-metal dielectric layer located between the first and second patterned layers of polycrystalline silicon.

8. The pre-metal dielectric structure of Claim 6, wherein the first patterned layer of polycrystalline silicon comprises a plurality of polycrystalline silicon islands.

9. The pre-metal dielectric structure of Claim 8, wherein the polycrystalline silicon islands are separated by spacing corresponding to the minimum design rule spacing.

10. The pre-metal dielectric structure of Claim 1, wherein the light-absorbing structure comprises amorphous silicon.

11. The pre-metal dielectric structure of Claim 1, wherein the first and second pre-metal dielectric layer comprise barrier films adjacent to the light-absorbing structure, wherein the barrier films suppress out-diffusion of impurities from other portions of the first and second pre-metal dielectric layer to the light-absorbing structure.

12. The pre-metal dielectric structure of Claim 1, further comprising one or more contact openings formed through the first and second pre-metal dielectric layers and the light-absorbing structure, wherein the contact openings expose one or more surfaces of the light-absorbing structure.

13. The pre-metal dielectric structure of Claim 12, further comprising sidewall dielectric material located on the one or more exposed surfaces of the light-absorbing structure.

14. A silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor comprising:

a semiconductor region having a first conductivity type;

a plurality of oxide-nitride-oxide (ONO) structures formed over the upper surface of the semiconductor region;

a plurality of word lines formed over the ONO structures, wherein each of the ONO structures is entirely covered by one of the word lines;

a first dielectric layer located over the plurality of word lines and the semiconductor region; and

light-absorbing sidewall spacers located over the first dielectric layer, and adjacent to sidewalls of the word lines.

15. The SONOS memory transistor of Claim 14, wherein the light-absorbing sidewall spacers comprise polycrystalline silicon.

16. The SONOS memory transistor of Claim 14, wherein the word lines comprise polycrystalline silicon.

17. The SONOS memory transistor of Claim 14, wherein the first dielectric layer comprises tetra-ethoxy-silane (TEOS).

18. A method of fabricating a fieldless array, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a surface of a semiconductor region;

patterning the ONO layer to create a first set of ONO structures that define locations for a plurality of diffusion bit lines of the fieldless array;

forming a plurality of word lines over the first set of ONO structures; and

patterning the first set of ONO structures, thereby creating a second set of ONO structures, wherein the second set of ONO structures are located entirely under the plurality of word lines,

forming a first dielectric layer over the word lines and the semiconductor region; and

forming light-absorbing sidewall spacers over the first dielectric layer and adjacent to sidewalls of the word lines.

19. The SONOS memory transistor of Claim 18, wherein the light-absorbing sidewall spacers comprise polycrystalline silicon.

20. The SONOS memory transistor of Claim 18, wherein the word lines comprise polycrystalline silicon.

21. The SONOS memory transistor of Claim 18, wherein the first dielectric layer comprises tetra-ethoxy-silane (TEOS).

22. A method for fabricating a pre-metal dielectric structure for a silicon-oxide-nitride-oxide-silicon (SONOS) memory transistor, the method comprising:

forming a first pre-metal dielectric layer over the SONOS memory transistor;

forming a light-absorbing structure over the first-pre-metal dielectric layer;

forming a second pre-metal dielectric layer over the light-absorbing structure; and

forming a first metal layer over the second pre-metal dielectric layer.

23. The method of Claim 22, further comprising forming a silicon nitride barrier film over the SONOS memory transistor and below the first pre-metal dielectric layer.

24. The method of Claim 22, wherein the light-absorbing structure is formed by depositing a first layer of polycrystalline silicon over the first pre-metal dielectric layer.

25. The method of Claim 24, further comprising the step of patterning the first polycrystalline silicon layer.

26. The method of Claim 25, wherein the light-absorbing structure is further formed by:

depositing an intermediate pre-metal dielectric layer over the patterned first polycrystalline silicon layer;

depositing a second layer of polycrystalline silicon over the intermediate pre-metal dielectric layer; and

patterning the second polycrystalline silicon layer.

27. The method of Claim 25, wherein the step of patterning comprises creating a plurality of polycrystalline silicon islands from the first polycrystalline silicon layer, wherein the spacing between the polycrystalline silicon islands corresponds to a minimum design rule spacing.

28. The method of Claim 22, further comprising forming one or more contact openings through the first and second pre-metal dielectric layers and the light-absorbing structure, wherein the contact openings expose one or more surfaces of the light-absorbing structure.

29. The method of Claim 28, further comprising forming sidewall dielectric material on the one or more exposed surfaces of the light-absorbing structure.